

## AMENDMENT TO THE CLAIMS

1. (Currently Amended) A method, comprising:  
receiving a command from a controller to access a memory in response to a memory request from a source;  
~~determining receiving, from the controller, the desired at least one of burst length~~  
~~information and~~ or latency information in association with based on the nature of  
~~the received command to access the memory~~ memory request; and  
providing data to or from the memory ~~in response to the command~~ based on at least one  
of the burst length information and the latency information.
2. (Original) The method of claim 1, wherein receiving a command comprises receiving at least one of a READ operation and WRITE operation to access the contents of the memory.
3. (Currently Amended) The method of claim 2, wherein ~~receiving~~ determining the latency information comprises receiving at least one of column address strobe latency information and write latency information.
4. Canceled.

5. (Currently Amended) The method of claim 1, wherein ~~receiving-determining the desired~~the burst length information comprises ~~receiving-determining a-the desired~~ burst length information based on an amount of data to be retrieved from the memory.

6. (Currently Amended) The method of claim 4, wherein ~~receiving the burst length information comprises receiving a burst length of a first pre-selected value in response to the controller receiving a request from a peripheral client and a burst length of a second pre-selected value in response to the controller receiving a request from a main client, wherein the first pre-selected value is less than the second pre-selected value~~determining the burst length information comprises determining the burst length information based on the source that provides the memory request.

7. (Currently Amended) The method of claim 1, wherein ~~receiving at least one of the burst length information and latency information~~providing the data comprises providing the data in response to receiving the burst length information or latency information over a redundant address line to the memory.

8. (Currently Amended) The method of claim 7, wherein ~~receiving the information over the redundant address line~~ comprises ~~receiving the information over a redundant row address line.~~

9. (Currently Amended) The method of claim 7, wherein ~~receiving the information over the redundant address line comprises receiving the information over a~~ redundant column address line.

10. (Currently Amended) An apparatus, comprising:  
a controller adapted to:

provide a command to access a memory array in response to a memory request from a source;

determine ~~provide~~ at least one of burst length information and latency information based on the nature of the memory request received from the source ~~in association with the command to access the memory array;~~ and  
receive data from the memory array ~~in response to the command~~ based on at least one of the burst length information and the latency information.

11. (Original) The apparatus of claim 10, wherein the controller is adapted to issue a READ operation access the contents of the memory.

12. (Currently Amended) The apparatus of claim 10, wherein the controller is adapted to provide at least one of the burst length information and the latency information ~~substantially~~ contemporaneously with the command to access the memory.

13. (Original) The apparatus of claim 10, wherein the controller is adapted to provide a burst length of a first pre-selected value in response to receiving a request from a

peripheral client and a burst length of a second pre-selected value in response to receiving a request from a main client, wherein the first pre-selected value is less than the second pre-selected value.

14. (Original) The apparatus of claim 10, wherein the controller is adapted to provide at least one of the burst length information and latency information over a redundant address line to the memory.

15. (Original) The apparatus of claim 14, wherein the controller is adapted to provide at least one of the burst length information and latency information over at least one of a redundant column address line and a redundant row address line.

16. (Currently Amended) The apparatus of claim 10, wherein the controller is adapted to issue a WRITE command and adapted to provide write latency information ~~substantially~~ contemporaneously with the WRITE command.

17. (Currently Amended) A system, comprising:

a memory array, and

a controller communicatively coupled to the memory array, the controller adapted to:

provide a command to access the memory array in response to a memory request from a source; and

~~determine provide~~ at least one of burst length information and latency information  
~~based on the nature of the received memory request in association with the~~  
~~command to access the memory array; and~~  
wherein the memory array is adapted to provide or receive data ~~in response to the~~  
~~command~~ based on at least one of the burst length information and the latency  
information.

18. (Original) The system of claim 17, wherein the controller is adapted to issue at least one of a READ operation and WRITE operation access the contents of the memory.

19. (Currently Amended) The system of claim 17, wherein the controller is adapted to provide at least one of the burst length information and the latency information ~~substantially contemporaneously~~ with the command to access the memory.

20. (Original) The system of claim 17, wherein the controller is adapted to provide a burst length of a first pre-selected value in response to receiving a request from a peripheral client and a burst length of a second pre-selected value in response to receiving a request from a main client, wherein the first pre-selected value is less than the second pre-selected value.

21. (Original) The system of claim 17, wherein the controller is adapted to provide at least one of the burst length information and latency information over a redundant address line to the memory.

22. (Currently Amended) An apparatus, comprising:

means for providing a command from a controller to access a memory in response to a memory request from a source;

means for ~~providing~~determining, from the controller, at least one of burst length information and or latency information based on the nature of the received memory request in association with the command to access the memory; and

means for providing data to or from the memory ~~in response to the command~~ based on at least one of the burst length information and the latency information.

23. (Currently Amended) An apparatus, comprising:

a memory adapted to:

receive a request ~~command from a memory controller~~ to access contents of the memory;

receive, from the memory controller, at least one of burst length information and latency information based on the nature of the memory request ~~in association with the command to access the contents~~; and

provide data from the memory ~~in response to the command~~ based on at least one of the burst length information and the latency information.

24. (Currently Amended) The apparatus of claim 23, wherein memory is adapted to receive at least one of the burst length information and the latency information ~~substantially contemporaneously~~ with the command to access the memory.

25. (Original) The apparatus of claim 23, wherein the memory is adapted to receive a burst length of a first pre-selected value in response to the controller receiving a request from a peripheral client and a burst length of a second pre-selected value in response to the controller receiving a request from a main client, wherein the first pre-selected value is less than the second pre-selected value.

26. (Original) The apparatus of claim 23, wherein the memory is adapted to receive at least one of the burst length information and latency information over a redundant address line.

27. (Original) The apparatus of claim 26, wherein the memory is adapted to receive at least one of the burst length information and latency information over at least one of a redundant column address line and a redundant row address line.

28. (Currently Amended) The apparatus of claim 23, wherein the memory is adapted to receive a WRITE command and adapted to receive write latency information ~~substantially~~ contemporaneously with the WRITE command.

29. (New) An apparatus, comprising:

a controller adapted to:

receive requests to access memory; and

access the memory using different burst lengths without requiring reprogramming of a

register holding information relating to burst length.